PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Basso et al.	)	Examiner:
Serial No.: To be assigned	)	Art Unit:
Filed: Herewith	)	
For: **STRUCTURE AND METHOD FOR SCHEDULER PIPELINE DESIGN FOR HIERARCHICAL LINK SHARING**	)	

Docket No.: RPS920030157US1 (IRA-10-5829)

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Information Disclosure Statement is being filed to fulfill the duty of candor and good faith toward the Patent and Trademark Office, as required pursuant to 37 C.F.R. § 1.56.

Listed on the attached PTO form 1449 is information known to persons substantively involved in the preparation of the application identified above, and that a reasonable Examiner would consider important when deciding whether to allow the application. This document is not to be construed as a representation that a search to locate the most relevant information has been made, nor a representation that more pertinent information does not exist.

Copies of information listed under "Foreign Patents" and "Other Documents" on the attached PTO Form 1449 are provided herewith.

The identification of any information herein is not intended to be, and should not be understood as being, an admission that such information, in fact, constitutes "prior art" within the meaning of applicable law. The "prior art" status of any information is a matter to be resolved during prosecution.

This Information Disclosure Statement is being filed concurrently with the application and, consequently, prior to an Office Action. Accordingly, it is not believed that any fee is required relating to the filing of this Information Disclosure Statement. If this is not the case, the Patent Office is hereby authorized to charge any related fee to Deposit Account No. 09-1990.

Respectfully submitted,

Date: January 29, 2004

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Attachments

Subst. Form PTO-1449 APPLICANT'S INFORMATION DISCLOSURE STATEMENT	Atty. Docket No.: RPS920030157US1 (IRA-20-5829)	Serial No.: To be assigned
	Applicant: Basso et al	
	Filing Date: Herewith	Group: To be assigned

U.S. PATENT DOCUMENTS

Initial*		Document No.	Date	Name	Class	Subcl.	Filing Date
	AA	5,835,745	11/10/1998	Sager et al	395	391	03/07/1996
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	AI	JP11203145A	07/30/1999	Japan			Abstract attached
	AJ	JP20022334126A	11/22/2002	Japan			Abstract attached

OTHER DOCUMENTS

	AK	IBM Technical Disclosure Bulletin, Vol. 36, No. 12, "Compute-Send-Receive -> Sequence Processing within the Multisequencing in a Single Instruction Stream Scheduler", December, 1993, pp 3-8
	AL	INSPEC – (Chatha et al; 1998) – two articles; (Wakabayashi et al; 1992); Chatha et al; 2001) Dave et al; 1998/1997) – two articles, 7 pages
	AM	"Efficient Longest Executable Path Search for Programs with Complex Flows and Pipeline Effects", Stappert et al, 2001, pp 132-140
	AN	"SCED: A Generalized Scheduling Policy for Guaranteeing Quality-of-Service", Sariowan et al, IEEE/ACM Transactions on Networking, Vol. 7, No. 5, October, 1999, pp 669-684
	AO	"RECOD: A Retiming Heuristic To Optimize Resource And Memory Utilization in HW/SW Codesigns", Chatha et al, Proceedings of the Sixth International Workshop on Hardware / Software Codesign, IEEE Computer Society et al, March 15-18, 1998, pp 139-143
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	AQ	"COHRA: Hardware-Software Co-Synthesis of Hierarchical Distributed Embedded System Architectures", Dave et al, Proceedings of the Eleventh International Conference on VLSI Design, VLSI Society of India, January 4-7, 1998, pp 347-354

Examiner:	Date Considered:

*EXAMINER: Initial if reference considered, whether or not citation is in conformation with MPEP 609; draw line through citation if in conformance and not considered. Include copy of this form with next communication to applicant.

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	AK	"A Synthesis Algorithm for Pipelined Data Paths with Conditional Module Sharing", Wakabayashi et al, 1992 IEEE International Symposium on Circuits and Systems, Volume 2 of 6, IEEE, May 10-13, 1992, pp 677-680
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